

AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 3, line 20, with the following rewritten paragraph:

1 Another approach as shown in Figure 5 4 is a delayed driving scheme
2 which reduces the variation of the drain node voltage. The input synchronization
3 is realized by using two traditional latches as implemented using switches 504,
4 506, 508, and 510 in front of the delayed driving block. As shown in Figure 6,
5 the crossing points are lower than the middle point $(V_H+V_L)/2$ for PMOS output
6 switches, 514 and 516; while the crossing points are higher than the middle point
7 $(V_H+V_L)/2$ for NMOS output switches, 302 and 304 of Figures 3 and 4.